REMARKS

Claims 33-46 are pending in this application. By this Amendment, claims 8, 9 and 15-32 are canceled. No new matter is added by this Amendment.

I. Information Disclosure Statement

In the May 18, 2005, Office Action, the Patent Office applied U.S. Patent No. 5,514,879 (Yamazaki) in rejecting the claims. However, Yamazaki was not listed as a reference under Form PTO-892 that was attached to the May 18, 2005, Office Action. Accordingly, in response to the May 18, 2005, Office Action, Applicant filed an Amendment on August 15, 2005, requesting that Yamazaki be listed on a new Form PTO-892 or that the Form PTO-892 that was included in the May 18 Office Action be revised to include Yamazaki. The Office Action has failed to include Yamazaki on any Form PTO-892. Accordingly, Applicant attaches hereto Form PTO-1449 including Yamazaki listed as a reference. Applicant respectfully requests that the Examiner acknowledge Yamazaki as having been considered and enter the Form PTO-1449 so that Yamazaki will be included on the Letters Patent once this application issues.

II. Election/Restrictions

The Office Action asserts that previously presented claims 21 and 23-29 are directed to non-elected subject matter. Applicant respectfully disagrees. Nonetheless, each of these claims is canceled, and as such, the Restriction Requirement is moot.

Furthermore, Applicant submits that new claims 31-46 are directed to the elected subject matter. That is, each of these claims read on Figs. 2A-3D.

III. Rejection Under 35 U.S.C. §112, First Paragraph

The Office Action rejects claims 31 and 32 under 35 U.S.C. §112, first paragraph. Claims 31 and 32 are herein canceled. Thus, this rejection is moot.

IV. Rejections Under 35 U.S.C. §102(b) and §103(a)

Claims 8, 9, 22 and 30 are rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,477,065 ("Nakagawa"); claims 8, 9, 16 and 30 are rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,294,824 ("Okada"); claims 17-20 are rejected under 35 U.S.C. §103(a) over either Nakagawa or Okada taken with U.S. Patent No. 5,016,986 ("Kawashima"); and claim 15 is rejected under 35 U.S.C. §103(a) over either Nakagawa or Okada taken with Kawashima. These rejections are respectfully traversed.

Claims 8, 9, 15-22 and 30 are herein canceled. Thus, with respect to these claims, this rejection is moot.

However, with respect to claims 33-35, as well as the claims depending therefrom, these claims are allowable in view of the applied references. In particular, each of claims 33-35 recite an intrinsic portion in the semiconductor film under a gate electrode. None of the applied references disclose this feature.

Instead, Nakagawa discloses a transistor having a semiconductor film that consists of a P-type region and an N-type region. However, Nakagawa does not disclose an intrinsic portion formed under a gate electrode, as recited in each of claims 33-35. Furthermore, Nakagawa also fails to disclose separating an impurity portion (a conductive type region) into two parts, as further disclosed in claim 33.

Okada discloses a transistor having a channel region under a conductive material 13 as a gate electrode. The channel region consists of a P-type region and an N-type region. However, Okada fails to disclose an intrinsic region formed under the gate electrode (conductive material 13), as recited in claims 33-35. Furthermore, Okada fails to disclose separating an impurity portion (a conductive type region) into two parts, as further recited by claim 33.

Kawashima fails to disclose an intrinsic region formed under a gate electrode, as recited in claims 33-35, and fails to disclose separating an impurity portion (a conductive type region) into two parts, as further recited in claim 33.

Furthermore, with respect to U.S. Patent No. 5,514,879 ("Yamazaki") that was previously applied in a previous Office Action, Yamazaki also fails to disclose an intrinsic region formed under a gate electrode, as recited by claims 33 and 35, and separating an impurity portion (conductive type region) into two parts, as further recited by claim 33. Instead, Yamazaki merely discloses a transistor having a channel region under gate electrode 40. The channel region consisting of a P-type region and an N-type region. See Fig. 7 of Yamazaki.

In summary, none of Nakagawa, Okada, Kawashima and/or Yamazaki disclose a relationship between an intrinsic portion and a conductive type portion under a gate electrode. Most specifically, none of the applied references disclose an intrinsic portion under a gate electrode, as recited in each of claims 33-35.

For the foregoing reasons, Nakagawa, Okada, Kawashima and/or Yamazaki, in any combination, fail to anticipate or otherwise render obvious the subject matter of claims 33-35, as well as the claims depending therefrom.

V. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the pending claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Linda M. Saltiel
Registration No. 51,122

JAO:LMS/eks

Attachment:
Request for Continued Examination

Date: January 13, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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